ADM-PCIE-9V8
User Manual

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1 Introduction

The ADM-PCIE-9V8 is an ultra-low latency high-performance reconfigurable computing card intended for low latency trading applications, featuring a screened AMD Virtex UltraScale+ Plus FPGA with low latency transceivers and four QSFP-DD cages.

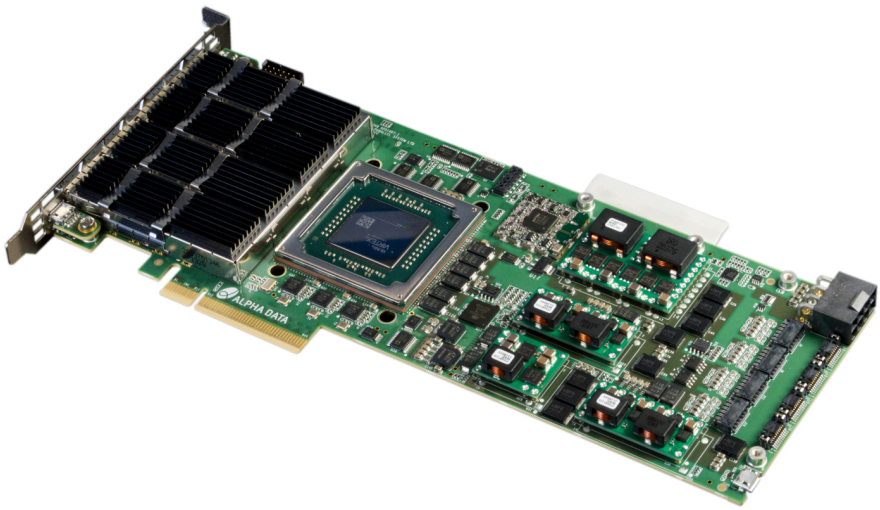

Figure 1 : ADM-PCIE-9V8 Product Photo

1.1 Key Features

Key Features

- Supports Virtex UltraScale+ Ultra Low Latency VU2P FPGA.
- Propagation delays between FPGA nad QSFP-DD cage as low as 60ps.
- PCIe Gen3 x8 capable
- Passive thermal management configuration
- 3/4 length, full profile, x8 edge PCIe form factor
- Four QSFP-DD cages for a total of 32 channels each capable of up to 25 Gpbs operation (total 800 Gbps)
- Four 4-lane FireFly connectors for a total of 16 channels each capable of up to 25 Gpbs operation (total 400 Gbps)
- Front panel and rear edge JTAG access via USB port
- FPGA configurable over USB/JTAG and SPI configuration flash
- Voltage, current, and temperature monitoring
- 8 GPIO signals and 1 isolated timing input
- User LEDs and timing input options.

1.2 Order Code

See https://www.alpha-data.com/product/adm-pcie-9v8/ for complete ordering options.

2 Board Information

2.1 Physical Specifications

The ADM-PCIE-9V8 complies with PCI Express CEM revision 3.0.

Description	Measure
PCB Dy	100.15 mm
Total Dx	239.0 mm
PCB Dz	1.6 mm

Table 1 : Mechanical Dimensions (PCB only)

Description	Measure
Total Dy	126.35 mm
Total Dx	252.2 mm
Total Dz	19.7 mm
Weight	600 grams (without QSFP-DD modules)

Table 2 : Mechanical Dimensions (Fully Assembled)

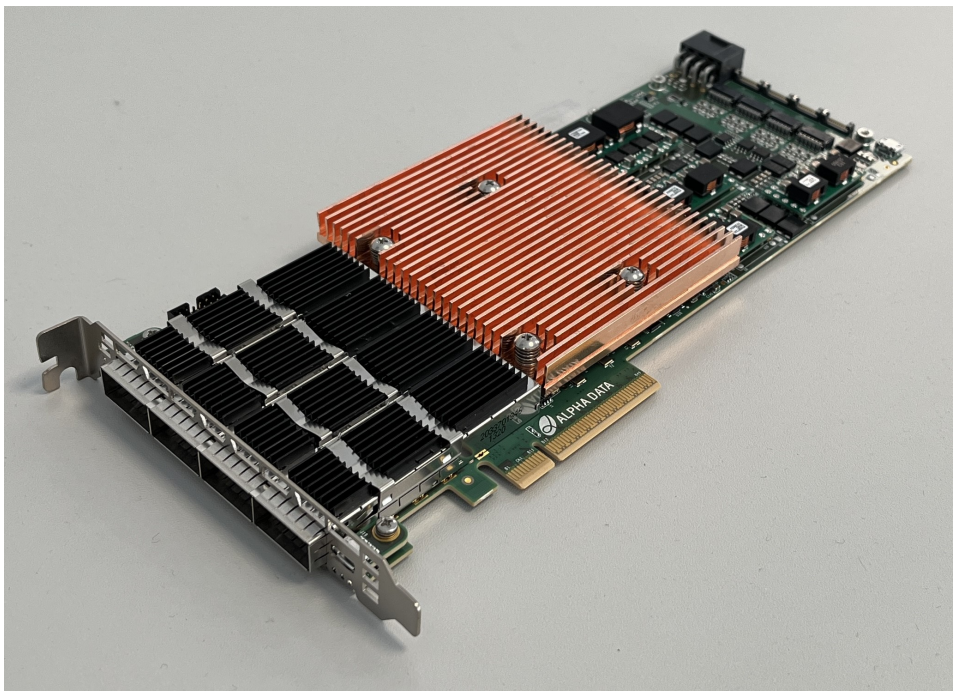

Figure 2 : ADM-PCIE-9V8 Fully Assembled

2.2 Chassis Requirements

2.2.1 PCI Express

The ADM-PCIE-9V8 is capable of PCIe Gen 3 with 8 lanes, using the AMD Integrated Block for PCI Express.

2.2.2 Mechanical Requirements

An 8 or 16 lane physical PCIe slot is required for mechanical compatibility.

2.2.3 Power Requirements

The ADM-PCIE-9V8 draws power from the PCIe Edge and the 6-pin ATX power connector. The ADM-PCIE-9V8 does not use or require the 3.3V power from the PCIe Edge (though it does use 3.3V AUX). It can operate with only the PCIe edge if desired. To operate with PCIe edge only, ensure SW1-3 is OFF (see Switches). As per PCIe specification, users should limit the board power consumption to 66W when using only the PCIe edge power. Adding the 6-pin ATX connector provides additional 75W of power, bringing the total board power dissipation maximum to 141W.

Power consumption estimation requires the use of the AMD XPE spreadsheet and a power estimator tool available from Alpha Data. Please contact **support@alpha-data.com** to obtain this tool.

The power available to the rails calculated using XPE are as follows:

Voltage	Source Name	Current Capability
0.85-0.90	VCC_INT + VCCINT_IO + VCC_BRAM	100A
0.9	MGTAVCC	16A
1.2	MGTAVTT	30A
1.8	VCCAUX + VCCAUX_IO + VCCO_1.8V	5A
1.8	MGTVCCAUX	2.5A
3.3	3.3V for Optics	30A

Table 3 : Available Power By Rail

2.3 Thermal Performance

If the FPGA core temperature exceeds 105 degrees Celsius, the FPGA design will be cleared to prevent the card from over-heating.

The ADM-PCIE-9V8 comes with a heat sink to help avoid thermal overstress of FPGA, since it is typically the hottest point on the card. The FPGA die temperature must remain under 100 degrees Celsius. To calculate the FPGA die temperature, take your application power, multiply by Theta JA from the table below, and add to your system internal ambient temperature.

The power dissipation can be estimated by using the Alpha Data power estimator in conjunction with the AMD Xilinx Power Estimator (XPE) downloadable at http://www.xilinx.com/products/technology/power/xpe.html. Download the UltraScale tool and set the device according to your part number details: Virtex UltraScale+, VU2P. Set the ambient temperature to your system ambient and select 'user override' for the effective theta JA and enter the figure associated with your system LFM in the blank field. Proceed to enter all applicable design elements and utilization in the following spreadsheet tabs. Next acquire the 9V5 power estimator from Alpha Data by contacting support@alpha-data.com. You will then plug in the FPGA power figures along with Optical module figures to get a board level estimate.

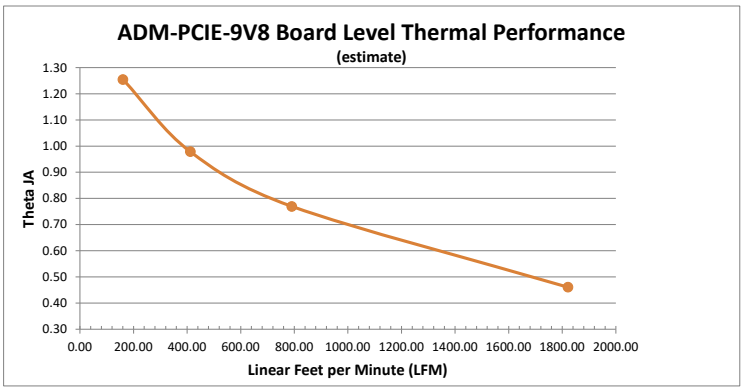

Figure 3 : Thermal Performance

2.4 Customizations

Alpha Data provides extensive customization options to existing commercial off-the-shelf (COTS) products. Some options include, but are not limited to: additional networking cages in adjacent slots, enhanced heat sinks, baffles, and circuit additions.

Please contact sales@alpha-data.com to get a quote and start your project today.

3 Functional Description

3.1 Overview

The ADM-PCIE-9V8 is a versatile reconfigurable computing platform with an Ultra Low Latency Virtex UltraScale+ VU2P FPGA, a Gen3x8 PCIe interface, four QSFP-DD cages, four Samtec FireFly connectors, an isolated input for a timing synchronization pulse, a 12 pin header for general purpose use (clocking, control pins, debug, etc.), front panel LEDs, and a robust system monitor.

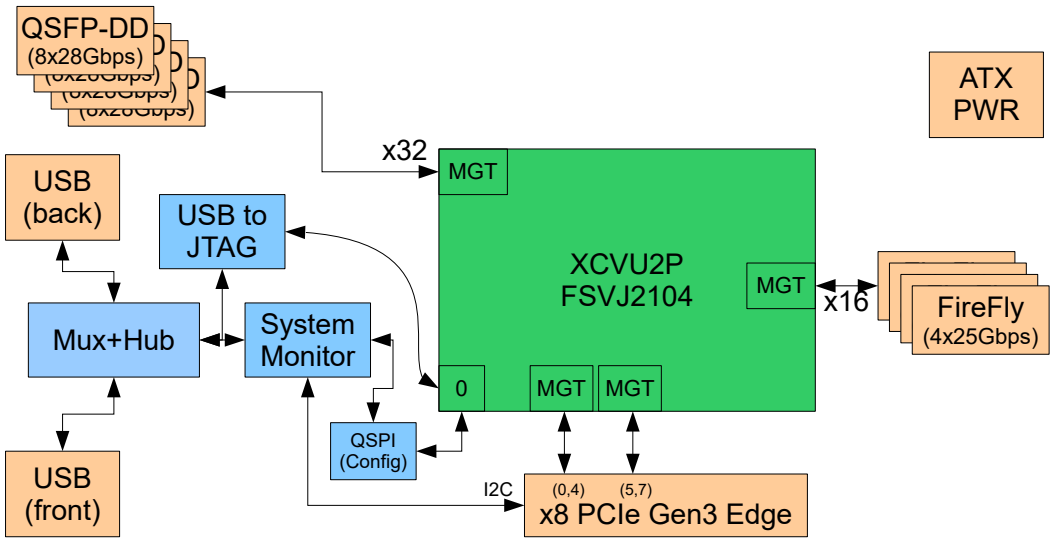

Figure 4 : ADM-PCIE-9V8 Block Diagram

3.1.1 Switches

The ADM-PCIE-9V8 has an octal DIP switch SW1, located on the rear side of the board. The function of each switch in SW1 is detailed below:

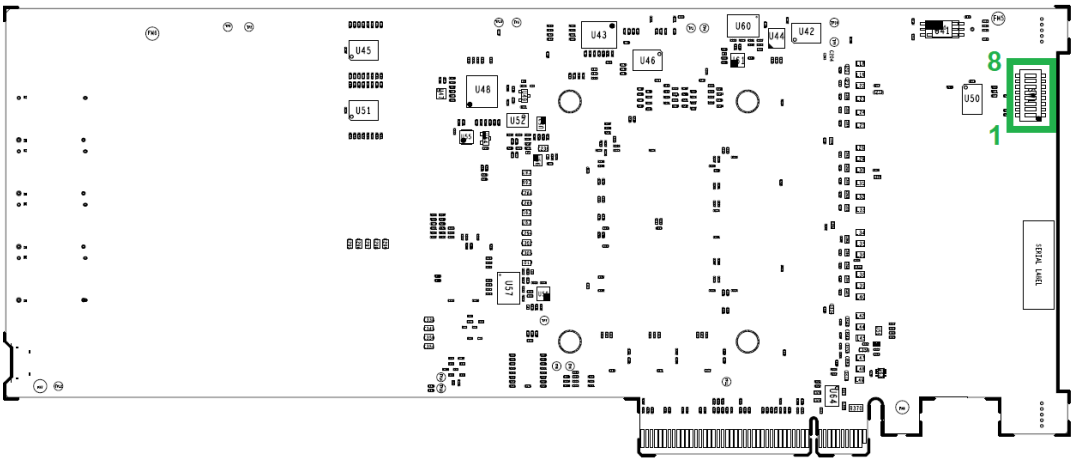

Figure 5 : Switches

Switch	Factory Default	Function	OFF State	ON State
SW1-1	OFF	User Switch 0	Pin AW33 = '1'	Pin BF52 = '0'
SW1-2	OFF	User Switch 1	Pin AY36 = '1'	Pin BF47 = '0'
SW1-3	ON	12V Auto-detect	12V PCIe edge auto-detect	ATX AUX power required
SW1-4	OFF	Power Off	Board will power up	Immediately power down
SW1-5	OFF	Service Mode	System Monitor normal operation	System Monitor Service Mode (firmware update etc.)
SW1-6	OFF	HOST_I2C_EN	System Monitor connected isolated from PCIe slot I2C	System Monitor connected to PCIe slot I2C
SW1-7	OFF	RESERVED	NA	NA
SW1-8	OFF	RESERVED	NA	NA

Table 4 : Switch Functions

Use I/O Standard "LVCMOS18" when constraining the User Switch pins.

3.1.2 LEDs

There are 9 LEDs on the ADM-PCIE-9V8, 6 of which are general purpose and whose meaning can be defined by the user. The other 3 have fixed functions described below:

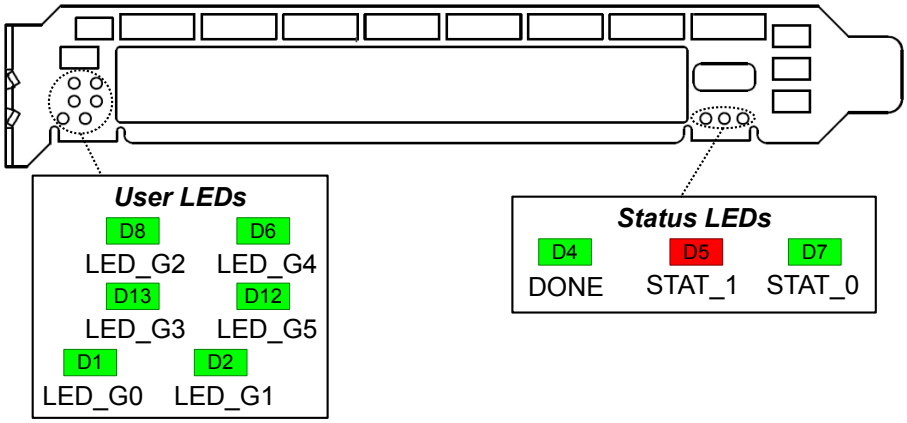

Figure 6 : Front Panel LEDs

Comp. Ref.	Function	ON State	OFF State
D1	USER_LED_G0_1V8	User defined '0'	User defined '1'
D2	USER_LED_G1_1V8	User defined '0'	User defined '1'
D8	USER_LED_G2_1V8	User defined '0'	User defined '1'
D11	USER_LED_G3_1V8	User defined '0'	User defined '1'
D10	USER_LED_G4_1V8	User defined '0'	User defined '1'
D12	USER_LED_G5_1V8	User defined '0'	User defined '1'
D6	DONE	FPGA is configured	FPGA is not configured
D7	Status 1	See Status LED Definitions	
D9	Status 0	See Status LED Definitions	

Table 5 : LED Details

See Section Complete Pinout Table for full list of user controlled LED nets and pins

3.2 Clocking

The ADM-PCIE-9V8 provides flexible reference clock solutions for the many multi-gigabit transceiver quads and FPGA fabric. The reprogrammable clocks from the LMK61E2 are reconfigurable from the front panel USB Interface by using Alpha Data's avr2util utility. This allows the user to configure almost any arbitrary clock frequency during application run time. The maximum clock frequency for the LMK61e2 is 900MHz. There is also an of embedding IP into the FPGA design that permits programmable clock re-configuration via PCIe or from within the FPGA.

There are four Si5324 jitter attenuators. These can provide clean and synchronous clocks to all of the QSFP and FireFly quad locations at many clock frequencies. The Si5324 can be reconfigured over I2C using a controller embedded in the FPGA design.

All clock names in the section below can be found in Complete Pinout Table.

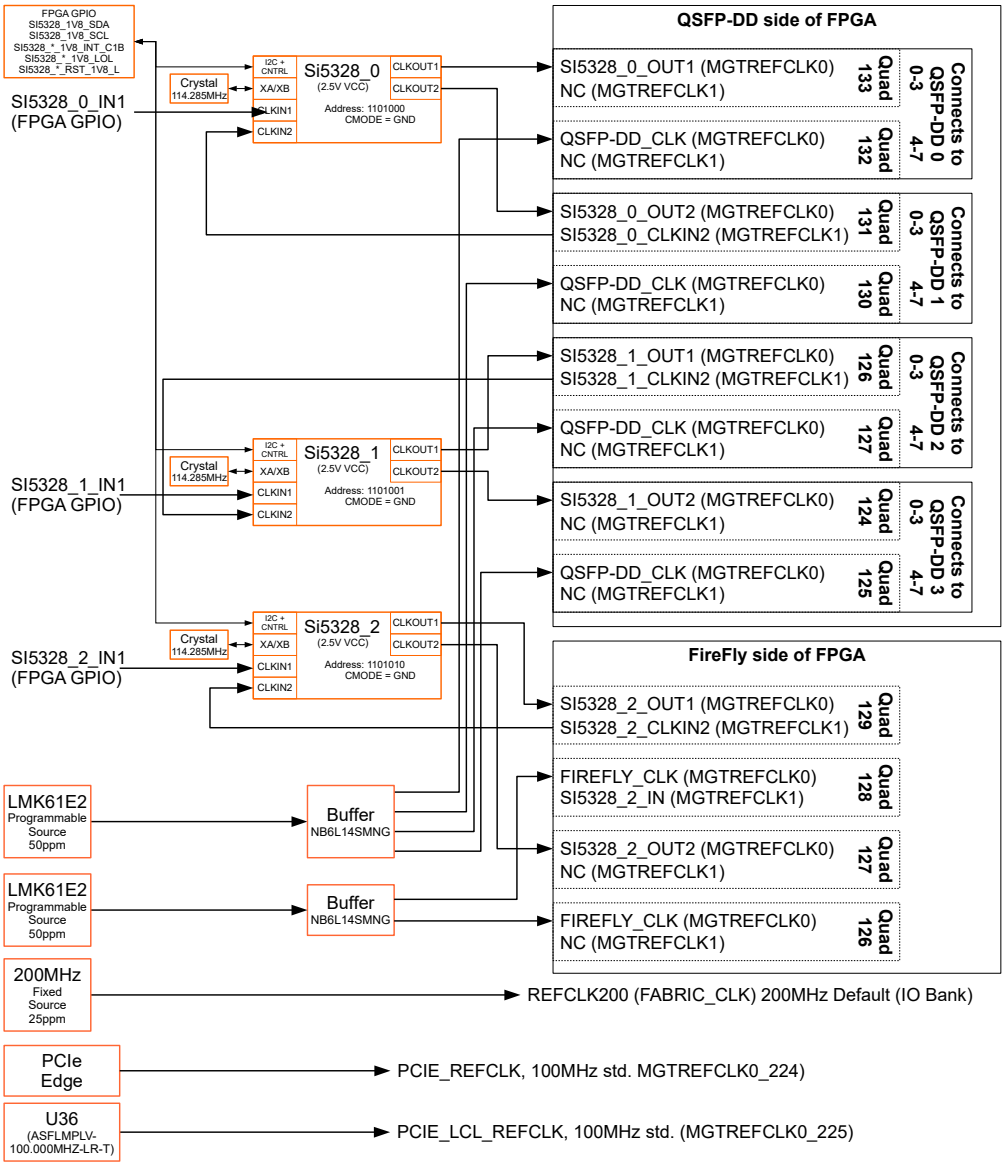

Figure 7 : Clock Topology

3.2.1 LMK61E2

The ADM-PA120 uses the LMK61E2 for arbitrary clock frequency synthesis. For complete technical details, please reference the datasheet:
https://www.ti.com/lit/ds/symlink/lmk61e2.pdf

The ADM-PA120 uses two LMK61E2 devices in the clock architecture. These can be accessed through either the USB or PCIe link using the AVR2UTIL application. See additional details on avr2util in the section: USB Interface.

To re-program the LMK61E2 in a non-volatile manner, issue the following command:

```
avr2util <other options> setclknv-regmap <clock#> <reg. map file>
```

> **Note:**
> Each LMK61E2 is rated for only 100 non-volatile write operations.

To re-program the LMK61E2 in a volatile manner, issue the following command:

```
avr2util <other options> setclk-regmap <clock#> <reg. map file>
```

<other options> should be left blank for PCIE, and '-usbcom' for USB.

<clock#> is 0 for MGT_PROGCLK and 1 for MEM_CLK.

<reg. map file> is a text file generated using the "LMK61xx Oscillator Programming Tool — SNAC074.ZIP" which can be obtained with a TI login from this page: https://www.ti.com/tool/LMK61E2EVM. After you have the tool installed, launch the application, type in the desired frequency, select "LVDS" output standard, click "Generate Configuration", then go to "File->Export hex register values"

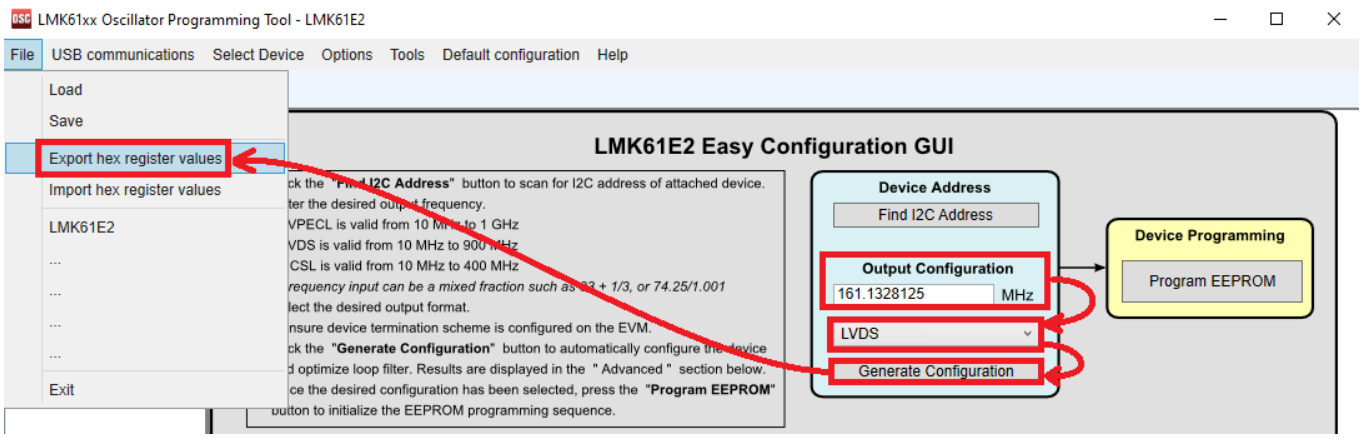

Figure 8 : LMK61xx Oscillator Programming Tool GUI

3.2.2 Si5324

Please note that some net names in the design refer to the SI5324 as an SI5328. These devices are footprint and functionally compatible. The SI5324E-C-GM was chosen at the time of production due to availability concerns and is the part fitted on every board. The Si5328 is not used.

If jitter attenuation is required please see the reference documentation for the Si5324.
www.skyworksinc.com/-/media/Skyworks/SL/documents/public/data-sheets/Si5324.pdf

There are two input clock options. Si5324 pin CLKIN1 (board net name SI5328_*_REFCLK_IN1_P/N) of the Si5324 is connected to a GPIO clock capable pin, allowing the application design to feed this clock from anywhere within the FPGA PL. Si5328 pin CLKIN2 (board net name SI5328_*_CLKIN2_P/N) of the Si5324 is connected to a MGT clock output for the most direct clock recovery architecture.

The two output clocks are connected to different quads to provide clocking capability to all quads on the entire FPGA.

The INT_C1B and LOL signals for the Si5324 are available for use, and can be located at net names SI5328_*_INT_C1B and SI5328_*_LOL in the Complete Pinout Table.

The active low reset of the Si5324 is accessible to the FPGA. See net names SI5328_*_RST_L in the Complete Pinout Table.

Note:
INT_C1B and LOL have an external pull-up resistor.

Note:
SI5328_*_RST_L has a pull-down and will be reset when the FPGA is cleared.

The Si5324 configuration register map is volatile, and must be written on each power up event or FPGA reconfiguration over I2C. Use nets SI5328_SDA and SI5328_SCL at pins located in the Complete Pinout Table. The Si5324 device is configured the I2C address shown in the table below:

device	7bit Hex Address	Binary Address
Si5328_0	68	110_1000
Si5328_1	69	110_1001
Si5328_2	6A	110_1010
Si5328_3	6B	110_1011

Table 6 : Si5324 address table

3.2.3 PCIe Reference Clocks

The 8 MGT lanes connected to the PCIe card edge use MGT tiles 224 through 225 and use the system 100 MHz clock (net name PCIE_REFCLK).

Alternatively, a clean, onboard 100MHz clock is available as well (net name PCIE_LCL_REFCLK).

3.2.4 Fabric Clock

The design offers a fabric clock (net name REFCLK200_PIN_P/N) which is 200 MHz. This clock is intended to be used for IDELAY elements in FPGA designs. The fabric clock is connected to a Global Clock (GC) pin.

External termination is included on the PCB.

3.2.5 Programming Clock (EMCCLK)

A 100MHz clock (net name EMCCLK_B) is fed into the EMCCLK pin to drive the SPI flash device during configuration of the FPGA. Note that this is not a global clock capable IO pin.

3.2.6 QSFP-DD Clock

The QSFP reference clock connects to one quad of each QSFP-DD connector. This programable clock has a default 161.1328125MHz reference clock. This clock frequency can be changed to any arbitrary clock frequency up to 900MHz by re-programming the LMK61E2 reprogrammable clock oscillator. See details on avr2util in the section: USB Interface.

See net names QSFP_CLK_* for pin locations.

The QSFP-DD cages are also located such that they can be clocked from the Si5324 jitter attenuators.

See net names SI5328_*_OUT_* for pin locations.

3.3 PCI Express

The ADM-PCIE-9V8 is capable of PCIe Gen 3 with 8 lanes. The FPGA drives these lanes directly using the Integrated PCI Express block from AMD. Negotiation of PCIe link speed and number of lanes used is generally automatic and does not require user intervention.

PCI Express reset (PERST#) connected to the FPGA through a buffer. See Complete Pinout Table signal PERST0_1V8_L.

The other pin assignments for the high speed lanes are provided in the pinout attached to the Complete Pinout Table

The PCI Express specification requires that all add-in cards be ready for enumeration within 120ms after power is valid (100ms after power is valid + 20ms after PERST is released). The ADM-PCIE-9V8 does meet this requirement when configured from a tandem bitstream with the proper SPI constraints detailed in the section: Configuration From Flash Memory. For more details on tandem configuration, see AMD xapp 1179.

Note:
Different motherboards/backplanes will benefit from different RX equalization schemes within the PCIe IP core provided by AMD. Alpha Data recommends using the following setting if a user experiences link errors or training issues with their system: within the IP core generator, change the mode to "Advanced" and open the "GT Settings" tab, change the "form factor driven insertion loss adjustment" from "Add-in Card" to "Chip-to-Chip" (See AMD PG195, PG213, and PG239 for more details).

3.4 QSFP-DD

Trace lengths for the QSFP links and the associated estimated propagation delay for each lane is listed in appendix Propagation Delays. These delays were calculated using the estimated propagation delay of Megtron 6 PCB laminate, which is 5.85ps/mm.

Four QSFP-DD cages are available at the front panel. These cages are capable of housing either QSFP28 or QSFP-DD cables (backwards compatible). Both active optical and passive copper QSFP-DD/QSFP28 compatible models are fully compliant. The communication interface can run at up to 25Gbps per channel. Each QSFP-DD cage has 8 channels (total maximum bandwidth of 200Gbps per cage). This cage is ideally suited for 8x 10G/25G, 2x 100G Ethernet, or any protocol supported by the AMD GTF Transceivers. Please see AMD User Guide UG1549 for more details on the capabilities of the transceivers.

All QSFP-DD cages have control signals connected to the FPGA. Their connectivity is detailed in the Complete Pinout Table at the end of this document. The notation used in the pin assignments is QSFP_0*, QSFP_1*, QSFP_2*, and QSFP_3*, with locations clarified in the diagram below.

The Management Interface of each QSFP-DD cage is connected to the FPGA, as detailed in Complete Pinout Table. The available signals are SDA/SCL (I2C), INT_L (interrupt), LPMODE (low power mode), RST_L (reset), and MODPRS_L (module present).

Note:
The LPMODE (Low Power Mode) to the cage is pulled down by default.

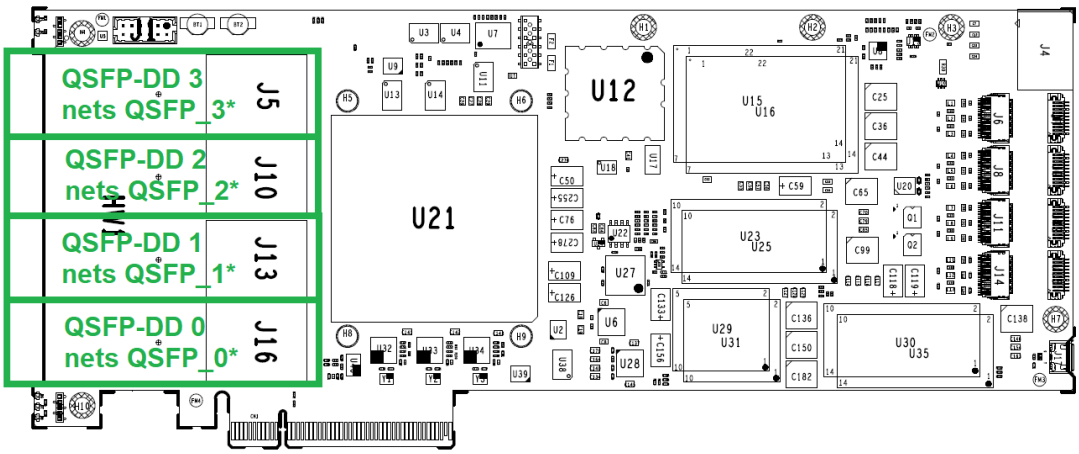

Figure 9 : QSFP-DD Location

3.5 FireFly

Trace lengths for the FireFly links and the associated estimated propagation delay for each lane is listed in appendix Propagation Delays. These delays were calculated using the estimated propagation delay of Megtron 6 PCB laminate, which is 5.85ps/mm.

There are four FireFly sites available on the circuit board. The sites are capable of hosting either active optical or passive copper FireFly connectors. The communication interface can run at up to 25Gbps per channel in either cable type. There are 16 channels on the FireFly site (total maximum bandwidth of 400Gbps). This site is ideally suited for 16x 10G/25G, 4x 100G Ethernet, or any other protocol supported by the Xilinx GTF Transceivers. Please see AMD User Guide UG1549 for more details on the capabilities of the transceivers.

All FireFly site have control signals connected to the ACAP. Their connectivity is detailed in the Complete Pinout Table at the end of this document. The notation used in the pin assignments is FIREFLY* with locations clarified in the diagram below.

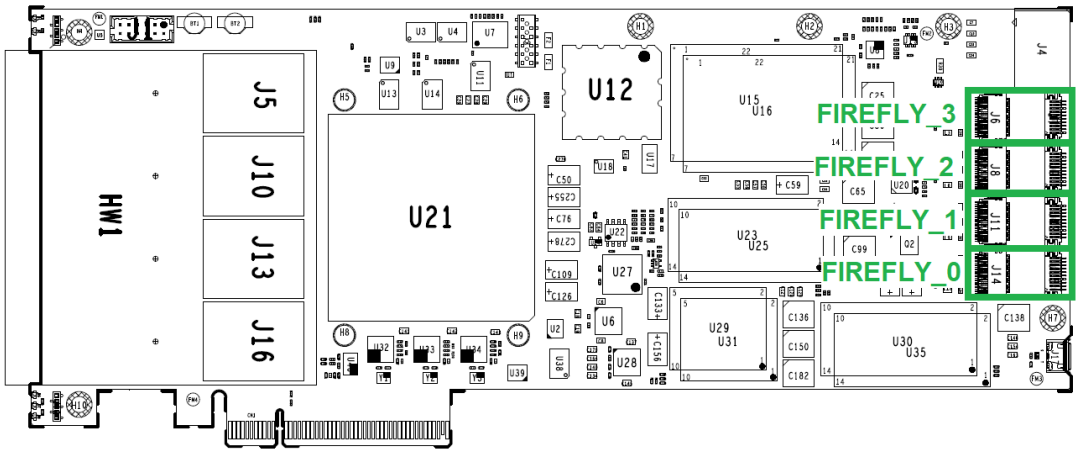

Figure 10 : FireFly Locations

The management interface of each FireFly module is connected directly to the FPGA. Each low speed sideband signals (MODPRS, INT_L, RST_L, SDA, SCL) has an external pull-up resistor.

3.6 System Monitor

The ADM-PCIE-9V8 has the ability to monitor its own temperature and the voltages and currents of certain power supply rails, in order to provide an indication of board health. The monitoring is implemented using an Atmel AVR microcontroller.

If the core FPGA temperature exceeds 105 degrees Celsius, the FPGA will be cleared to prevent damage to the card.

The microcontroller monitors power supply rail voltages & currents and temperatures at certain points on the board. This information can be read out via USB using the avr2util utility, and also via PCIe if RD-9V8 is purchased.

Monitors	Identifier	Purpose/Description
ETC	ETC	Elapsed time counter (seconds)
EC	EC	Event counter (power cycles)
12V_AUX	ADC00	12v board input supply from 6-pin ATX Cable
12V_AUX_I	ADC01	12V input current from 6-pin ATX Cable in amps
12V_EDGE	ADC02	12V board input supply from PCIe Edge
12V_EDGE_I	ADC03	12V board input current from PCIe Edge in amps
3V3_EDGE	ADC04	3.3V board input supply from PCIe edge (unused)
3V3_AUX	ADC05	3.3V auxilary board input supply from PCIE edge
3V3_DIG	ADC06	3.3V generated onboard for QSFP optics
2V5_CLK	ADC07	2.5V generated onboard for clock circuitry
1V8_DIG	ADC08	1.8V generated onboard fpr FPGA IO voltage (VCCO)
1V8_MGT_AUX	ADC09	1.8V generated onboard for transceiver power (AVCC_AUX)
1V2_AVTT	ADC10	1.2V generated onboard for transceiver Power (AVTT)
0V9_AVCC	ADC11	0.9V generated onboard for transceiver Power (AVCC)
VCC_INT	ADC12	0.85-0.90V generated onboard for VccINT + VccBRAM + VccINT_IO
GND	ADC13	0V electrical ground
uC_Temp	TMP00	uC on-die temperature
Board0_Temp	TMP01	Board temperature near front panel (U3)
Board1_Temp	TMP02	Board temperature near back edge (U23)
FPGA_Temp	TMP03	FPGA on-die temperature

Table 7 : Voltage, Current, and Temperature Monitors

3.6.1 System Monitor Status LEDs

LEDs D7 (Red) and D9 (Green) indicate the card health status.

LEDs	*Status*
Green	Running and no alarms
Green + Red	Standby (Powered off)
Flashing Green + Flashing Red (together)	Attention - critical alarm active
Flashing Green + Flashing Red (alternating)	Service Mode
Flashing Green + Red	Attention - alarm active
Red	Missing application firmware or invalid firmware
Flashing Red	FPGA configuration cleared to protect board

Table 8 : Status LED Definitions

3.7 USB Interface

The FPGA can be configured directly from the USB connection on either the front panel or the rear card edge. The ADM-PCIE-9V8 utilizes the Digilent USB-JTAG converter box which is supported by the AMD software tool suite. Simply connect a micro-USB AB type cable between the ADM-PCIE-9V8 USB port and a host computer with Vivado installed. Vivado Hardware Manager will automatically recognize the FPGA and allow you to configure the FPGA and the SPI configuration Flash memory.

The same USB connector is used to directly access the system monitor system. All voltages, currents, temperatures, and non-volatile clock configuration settings can be accessed using Alpha Data's avr2util software at this interface.

Avr2util for Windows and the associated USB driver is downloadable here:
https://support.alpha-data.com/pub/firmware/utilities/windows/

Avr2util for Linux is downloadable here:
https://support.alpha-data.com/pub/firmware/utilities/linux/

Use "avr2util.exe /?" to see all options.

For example "avr2util.exe /usbcom com4 display-sensors" will display all sensor values.

Change 'com4' to match the com port number assigned under windows device manager.

3.8 Configuration

There are two main ways of configuring the FPGA on the ADM-PCIE-9V8:

- From Flash memory, at power-on, as described in Section 3.8.1
- Using USB cable connected at either USB port Section 3.8.2

3.8.1 Configuration From Flash Memory

The FPGA can be automatically configured at power-on from two 1 Gbit QSPI flash memory device configured as an x8 SPI device (Micron part numbers MT25QU01GBBB8E12-0). These flash devices are typically divided into two regions of 128 MiByte each, where each region is sufficiently large to hold an uncompressed bitstream for a VU2P FPGA.

The ADM-PCIE-9V8 is shipped with a simple PCIe endpoint bitstream which should be visible to the operating system (using e.g. Windows Device Manager or “lspci” in Linux) in order to provided confidence that the card is working correctly when installed in a system. On request, Alpha Data can pre-load custom bitstreams during production test. Please contact sales@alpha-data.com in order to discuss this possibility.

It is possible to use Multiboot with a fallback image on this hardware. The master SPI configuration interface and the Fallback MultiBoot are discussed in detail in Xilinx UG570.

At power-on, the FPGA attempts to configure itself automatically in SPI master mode, depending on the header of the bitstream that has been flashed into the card. This normally results in SPIx8 configuration at EMCCLK frequency. The configuration scheme used in the ADM-PCIE-9V5 is compatible with Multiboot; see Xilinx UG570 for details. The FPGA can also be made to reconfigure itself from an arbitrary Flash address using the ICAPE3 primitive; this is also described in Xilinx UG570.

The image loaded can also support tandem PROM or tandem PCIE with field update configuration methods. These options reduce power-on load times to help meet the PCIe reset timing requirements. Tandem with field also enables a host system to reconfigure the user FPGA logic without losing the PCIe link, a useful feature when system resets and power cycles are not an option.

The Alpha Data System Monitor is also capable of reconfiguring the flash memory and reprograming the FPGA. This provides a useful failsafe mechanism to re-program the FPGA even if it drops off the PCIe bus. The system monitor can be accessed with avr2util over USB at the front panel and rear edge.

3.8.1.1 Building and Programming Configuration Images

Generate a bitfile with these constraints (see xapp1233):

- set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
- set_property BITSTREAM.CONFIG.EXTMASTERCCLK_EN {DIV-1} [current_design]
- set_property BITSTREAM.CONFIG.SPI_32BIT_ADDR YES [current_design]
- set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 8 [current_design]
- set_property BITSTREAM.CONFIG.SPI_FALL_EDGE YES [current_design]
- set_property BITSTREAM.CONFIG.UNUSEDPIN {Pullnone} [current_design]
- set_property CFGBVS GND [current_design]
- set_property CONFIG_VOLTAGE 1.8 [current_design]
- set_property BITSTREAM.CONFIG.OVERTEMPSHUTDOWN Enable [current_design]

Generate an MCS file with these properties (write_cfgmem):

- -format MCS
- -size 256
- -interface SPIx8
- -loadbit "up 0x0000000 <directory/to/file/filename.bit>" (0th location)

Program with Vivado hardware manager with these settings (see xapp1233):

- SPI part: mt25qu01g-spi-x1_x2_x4_x8
- State of non-config mem I/O pins: Pull-none

3.8.2 Configuration via JTAG

A micro-USB AB Cable may be attached to the front panel or rear edge USB port. This permits the FPGA to be reconfigured using the Xilinx Vivado Hardware Manager via the integrated Digilent JTAG converter box. The device will be automatically recognized in Vivado Hardware Manager.

For more detailed instructions, please see “Using a Vivado Hardware Manager to Program an FPGA Device” section of Xilinx UG908: https://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_1/ug908-vivado-programming-debugging.pdf

3.9 GPIO Connector

The GPIO option consists of a versatile shrouded connector from Molex with part number 87832-1222. This connector gives users eight signals connected to the FPGA.

Recommended mating plug: Molex 0875681273 or 0511101260

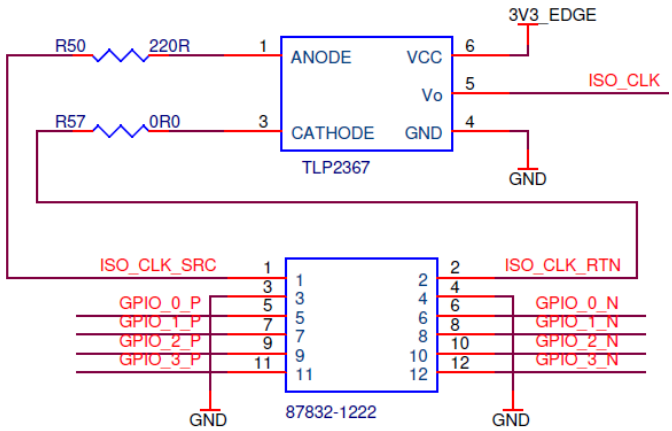

Figure 11 : GPIO Connector Schematic

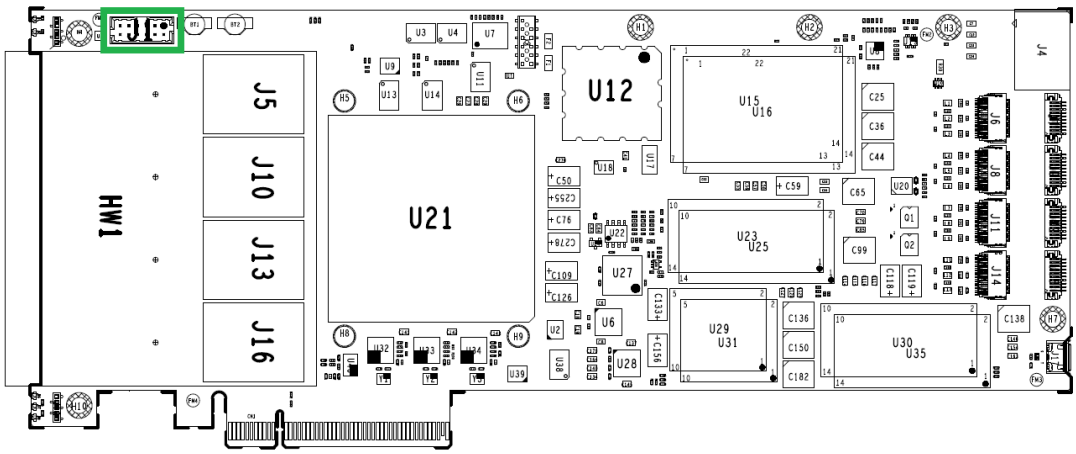

Figure 12 : GPIO Connector Location

3.9.1 Direct Connect FPGA Signals

8 nets are broken out to the GPIO header, as four sets of differential pairs. These signal are suitable for any 1.8V signalling standards supported by the Xilinx UltraScale architecture. See Xilinx UG571 for IO options. LVDS and 1.8 CMOS are popular options. The 0th GPIO signal index is suitable for a global clock connection.

The direct connect GPIO signals are limited to 1.8V by a quickswitch (74CBTLVD3245PW) in order to protect the FPGA from overvoltage on IO pins. This quickswitch allows the signals to travel in either direction with only 4 ohms of series impedance and less than 1ns of propagation delay. The nets are directly connected to the FPGA after the quickswitch.

Direct connect signal names are labelled GPIO_0_1V8_P/N and GPIO_1_1V8_P/N, etc. to show polarity and grouping. The signal pin allocations can be found in Complete Pinout Table

3.9.2 Timing Input

Pins 1 and 2 of J1 can be used as an isolated timing input signal (up to 25MHz). Applications can either directly connect to the GPIO connector, or Alpha Data can provide a cabled solution with an SMA or similar connector on the front panel. Contact sales@alpha-data.com for front panel connector options.

For pin locations, see signal name ISO_CLK in Complete Pinout Table.

The signal is isolated through a optical isolator part number TLP2367 with 220 ohm of series resistance.

3.10 User EEPROM

A 2Kb I2C user EEPROM is provided for storing MAC addresses or other user information. The EEPROM is part number CAT34C02HU4IGT4A

The address pins A2, A1, and A0 are all strapped to a logical '0'.

Write protect (WP), Serial Clock (SCL), and Serial Data (SDA) pin assignments can be found in Complete Pinout Table with the names SPARE_WP, SPARE_SCL, and SPARE_SDA respectively.

WP, SDA, and SCL signals all have external pull-up resistors on the card.

Appendix A: Propagation Delays

Trace Delay (ps)	Trace Length (mm)	Pin Number	Signal Name	Pin Name
52.9	9.0	L46	QSFP_1_RX3_N	MGTFRXN3_131
53.1	9.1	L45	QSFP_1_RX3_P	MGTFRXP3_131
55.6	9.5	AL45	QSFP_2_RX3_P	MGTFRXP3_126
55.6	9.5	AL46	QSFP_2_RX3_N	MGTFRXN3_126
66.1	11.3	BA45	QSFP_3_RX1_P	MGTFRXP1_124
66.3	11.3	BA46	QSFP_3_RX1_N	MGTFRXN1_124
66.4	11.4	N45	QSFP_1_RX1_P	MGTFRXP1_131
66.5	11.4	N46	QSFP_1_RX1_N	MGTFRXN1_131
71.7	12.3	AJ45	QSFP_2_RX5_P	MGTFRXP1_127
71.7	12.3	AJ46	QSFP_2_RX5_N	MGTFRXN1_127
73.9	12.6	AN46	QSFP_2_RX1_N	MGTFRXN1_126
74.0	12.7	AN45	QSFP_2_RX1_P	MGTFRXP1_126
81.5	13.9	R45	QSFP_1_RX7_P	MGTFRXP3_130
81.5	13.9	R46	QSFP_1_RX7_N	MGTFRXN3_130
85.2	14.6	AG46	QSFP_2_RX7_N	MGTFRXN3_127
85.6	14.6	AG45	QSFP_2_RX7_P	MGTFRXP3_127
88.0	15.0	AW46	QSFP_3_RX3_N	MGTFRXN3_124
88.4	15.1	AW45	QSFP_3_RX3_P	MGTFRXP3_124
96.1	16.4	AU45	QSFP_3_RX5_P	MGTFRXP1_125
96.1	16.4	AU46	QSFP_3_RX5_N	MGTFRXN1_125
100.2	17.1	AP39	QSFP_2_TX2_N	MGTFTXN2_126
100.3	17.1	AP38	QSFP_2_TX2_P	MGTFTXP2_126
101.1	17.3	AT39	QSFP_2_TX0_N	MGTFTXN0_126
101.2	17.3	AT38	QSFP_2_TX0_P	MGTFTXP0_126
106.4	18.2	C40	QSFP_0_TX6_P	MGTFTXP2_133
106.8	18.3	C41	QSFP_0_TX6_N	MGTFTXN2_133
109.2	18.7	AK44	QSFP_2_RX4_N	MGTFRXN0_127
109.2	18.7	AK43	QSFP_2_RX4_P	MGTFRXP0_127
109.5	18.7	BC46	QSFP_3_RX0_N	MGTFRXN0_124
109.7	18.8	U46	QSFP_1_RX5_N	MGTFRXN1_130
109.7	18.8	BC45	QSFP_3_RX0_P	MGTFRXP0_124
109.9	18.8	U45	QSFP_1_RX5_P	MGTFRXP1_130
112.0	19.1	T39	QSFP_1_TX0_N	MGTFTXN0_131

Table 9 : Complete Pinout Table (continued on next page)

Trace Delay (ps)	Trace Length (mm)	Pin Number	Signal Name	Pin Name
112.4	19.2	T38	QSFP_1_TX0_P	MGTFTXP0_131
113.7	19.4	V39	QSFP_1_TX6_N	MGTFTXN2_130
113.8	19.4	V38	QSFP_1_TX6_P	MGTFTXP2_130
114.0	19.5	AH43	QSFP_2_RX6_P	MGTFRXP2_127
114.2	19.5	AH44	QSFP_2_RX6_N	MGTFRXN2_127
115.0	19.7	G40	QSFP_0_TX4_P	MGTFTXP0_133
115.0	19.7	G41	QSFP_0_TX4_N	MGTFTXN0_133
116.1	19.9	T43	QSFP_1_RX6_P	MGTFRXP2_130
116.2	19.9	Y38	QSFP_1_TX4_P	MGTFTXP0_130
116.2	19.9	Y39	QSFP_1_TX4_N	MGTFTXN0_130
116.4	19.9	T44	QSFP_1_RX6_N	MGTFRXN2_130
118.3	20.2	P39	QSFP_1_TX2_N	MGTFTXN2_131
118.4	20.2	P38	QSFP_1_TX2_P	MGTFTXP2_131
119.4	20.4	AR46	QSFP_3_RX7_N	MGTFRXN3_125
119.5	20.4	AR45	QSFP_3_RX7_P	MGTFRXP3_125
119.9	20.5	U41	QSFP_1_TX7_N	MGTFTXN3_130
120.0	20.5	B44	QSFP_0_RX7_N	MGTFRXN3_133
120.3	20.6	B43	QSFP_0_RX7_P	MGTFRXP3_133
120.4	20.6	U40	QSFP_1_TX7_P	MGTFTXP3_130
123.6	21.1	W41	QSFP_1_TX5_N	MGTFTXN1_130
123.8	21.2	W40	QSFP_1_TX5_P	MGTFTXP1_130
126.3	21.6	A40	QSFP_0_TX7_P	MGTFTXP3_133
126.3	21.6	A41	QSFP_0_TX7_N	MGTFTXN3_133
127.1	21.7	E40	QSFP_0_TX5_P	MGTFTXP1_133
127.1	21.7	E41	QSFP_0_TX5_N	MGTFTXN1_133
127.5	21.8	BF43	QSFP_3_TX0_N	MGTFTXN0_124
127.6	21.8	BF42	QSFP_3_TX0_P	MGTFTXP0_124
127.9	21.9	AM43	QSFP_2_RX2_P	MGTFRXP2_126
128.1	21.9	AM44	QSFP_2_RX2_N	MGTFRXN2_126
128.6	22.0	G45	QSFP_0_RX3_P	MGTFRXP3_132
128.6	22.0	BD42	QSFP_3_TX2_P	MGTFTXP2_124
128.8	22.0	G46	QSFP_0_RX3_N	MGTFRXN3_132
128.9	22.0	BD43	QSFP_3_TX2_N	MGTFTXN2_124
131.5	22.5	AV44	QSFP_3_RX4_N	MGTFRXN0_125
131.5	22.5	AV43	QSFP_3_RX4_P	MGTFRXP0_125
131.6	22.5	M43	QSFP_1_RX2_P	MGTFRXP2_131

Table 9 : Complete Pinout Table (continued on next page)

Trace Delay (ps)	Trace Length (mm)	Pin Number	Signal Name	Pin Name
131.7	22.5	M44	QSFP_1_RX2_N	MGTFRXN2_131
132.9	22.7	AK39	QSFP_2_TX6_N	MGTFTXN2_127
133.0	22.7	AM38	QSFP_2_TX4_P	MGTFTXP0_127
133.0	22.7	AM39	QSFP_2_TX4_N	MGTFTXN0_127
133.1	22.8	AK38	QSFP_2_TX6_P	MGTFTXP2_127
136.0	23.2	V44	QSFP_1_RX4_N	MGTFRXN0_130
136.2	23.3	V43	QSFP_1_RX4_P	MGTFRXP0_130
136.8	23.4	M39	QSFP_0_TX0_N	MGTFTXN0_132
136.9	23.4	M38	QSFP_0_TX0_P	MGTFTXP0_132
138.1	23.6	AJ41	QSFP_2_TX7_N	MGTFTXN3_127
138.5	23.7	AJ40	QSFP_2_TX7_P	MGTFTXP3_127
140.0	23.9	K39	QSFP_0_TX2_N	MGTFTXN2_132
140.1	24.0	K38	QSFP_0_TX2_P	MGTFTXP2_132
142.5	24.4	AL40	QSFP_2_TX5_P	MGTFTXP1_127
142.6	24.4	AL41	QSFP_2_TX5_N	MGTFTXN1_127
144.2	24.6	AN41	QSFP_2_TX3_N	MGTFTXN3_126
144.2	24.7	AN40	QSFP_2_TX3_P	MGTFTXP3_126
148.0	25.3	D43	QSFP_0_RX6_P	MGTFRXP2_133
148.1	25.3	D44	QSFP_0_RX6_N	MGTFRXN2_133
149.0	25.5	E46	QSFP_0_RX5_N	MGTFRXN1_133
149.1	25.5	E45	QSFP_0_RX5_P	MGTFRXP1_133
152.1	26.0	P43	QSFP_1_RX0_P	MGTFRXP0_131
152.3	26.0	P44	QSFP_1_RX0_N	MGTFRXN0_131
152.4	26.1	AT44	QSFP_3_RX6_N	MGTFRXN2_125
152.6	26.1	J45	QSFP_0_RX1_P	MGTFRXP1_132
152.6	26.1	AT43	QSFP_3_RX6_P	MGTFRXP2_125
152.7	26.1	J46	QSFP_0_RX1_N	MGTFRXN1_132
152.9	26.1	AR40	QSFP_2_TX1_P	MGTFTXP1_126
152.9	26.1	AR41	QSFP_2_TX1_N	MGTFTXN1_126
153.6	26.3	N40	QSFP_1_TX3_P	MGTFTXP3_131
153.7	26.3	N41	QSFP_1_TX3_N	MGTFTXN3_131
159.5	27.3	R41	QSFP_1_TX1_N	MGTFTXN1_131
159.7	27.3	R40	QSFP_1_TX1_P	MGTFTXP1_131
160.0	27.4	AY44	QSFP_3_RX2_N	MGTFRXN2_124
160.2	27.4	AY43	QSFP_3_RX2_P	MGTFRXP2_124
160.8	27.5	L41	QSFP_0_TX1_N	MGTFTXN1_132

Table 9 : Complete Pinout Table (continued on next page)

Trace Delay (ps)	Trace Length (mm)	Pin Number	Signal Name	Pin Name
160.9	27.5	L40	QSFP_0_TX1_P	MGTFTXP1_132
161.5	27.6	BB43	QSFP_3_TX4_N	MGTFTXN0_125
161.8	27.7	BB42	QSFP_3_TX4_P	MGTFTXP0_125
166.2	28.4	J40	QSFP_0_TX3_P	MGTFTXP3_132
166.2	28.4	J41	QSFP_0_TX3_N	MGTFTXN3_132
166.7	28.5	AP43	QSFP_2_RX0_P	MGTFRXP0_126
166.9	28.5	AP44	QSFP_2_RX0_N	MGTFRXN0_126
172.7	29.5	AW40	QSFP_3_TX6_P	MGTFTXP2_125
172.7	29.5	AW41	QSFP_3_TX6_N	MGTFTXN2_125
179.6	30.7	BC40	QSFP_3_TX3_P	MGTFTXP3_124
179.7	30.7	BC41	QSFP_3_TX3_N	MGTFTXN3_124
181.2	31.0	H43	QSFP_0_RX2_P	MGTFRXP2_132
181.5	31.0	H44	QSFP_0_RX2_N	MGTFRXN2_132
187.1	32.0	AU41	QSFP_3_TX7_N	MGTFTXN3_125
187.3	32.0	AU40	QSFP_3_TX7_P	MGTFTXP3_125
188.9	32.3	BE40	QSFP_3_TX1_P	MGTFTXP1_124
188.9	32.3	BE41	QSFP_3_TX1_N	MGTFTXN1_124
189.3	32.4	F43	QSFP_0_RX4_P	MGTFRXP0_133
189.4	32.4	F44	QSFP_0_RX4_N	MGTFRXN0_133
194.1	33.2	BA40	QSFP_3_TX5_P	MGTFTXP1_125
194.2	33.2	BA41	QSFP_3_TX5_N	MGTFTXN1_125
211.5	36.2	K44	QSFP_0_RX0_N	MGTFRXN0_132
211.7	36.2	K43	QSFP_0_RX0_P	MGTFRXP0_132
630.5	107.8	W2	FIREFLY_0_RX3_P	MGTFRXP3_229
630.6	107.8	W1	FIREFLY_0_RX3_N	MGTFRXN3_229
635.3	108.6	AA1	FIREFLY_0_RX1_N	MGTFRXN1_229
635.3	108.6	AA2	FIREFLY_0_RX1_P	MGTFRXP1_229
637.1	108.9	AC1	FIREFLY_1_RX3_N	MGTFRXN3_228
637.2	108.9	AC2	FIREFLY_1_RX3_P	MGTFRXP3_228
638.0	109.1	AE1	FIREFLY_1_RX1_N	MGTFRXN1_228
638.3	109.1	AE2	FIREFLY_1_RX1_P	MGTFRXP1_228
638.5	109.1	AG2	FIREFLY_2_RX3_P	MGTFRXP3_227
638.6	109.2	AG1	FIREFLY_2_RX3_N	MGTFRXN3_227
644.3	110.1	AJ2	FIREFLY_2_RX1_P	MGTFRXP1_227
644.4	110.1	AJ1	FIREFLY_2_RX1_N	MGTFRXN1_227
669.3	114.4	AL1	FIREFLY_3_RX3_N	MGTFRXN3_226

Table 9 : Complete Pinout Table (continued on next page)

Trace Delay (ps)	Trace Length (mm)	Pin Number	Signal Name	Pin Name
669.4	114.4	AB3	FIREFLY_0_RX0_N	MGTFRXN0_229
669.5	114.4	AL2	FIREFLY_3_RX3_P	MGTFRXP3_226
669.6	114.5	AB4	FIREFLY_0_RX0_P	MGTFRXP0_229
671.4	114.8	AD4	FIREFLY_1_RX2_P	MGTFRXP2_228
671.5	114.8	AD3	FIREFLY_1_RX2_N	MGTFRXN2_228
672.6	115.0	AN1	FIREFLY_3_RX1_N	MGTFRXN1_226
672.7	115.0	AN2	FIREFLY_3_RX1_P	MGTFRXP1_226
676.0	115.6	AF4	FIREFLY_1_RX0_P	MGTFRXP0_228
676.1	115.6	AF3	FIREFLY_1_RX0_N	MGTFRXN0_228
677.9	115.9	AK3	FIREFLY_2_RX0_N	MGTFRXN0_227
678.1	115.9	Y3	FIREFLY_0_RX2_N	MGTFRXN2_229
678.2	115.9	AK4	FIREFLY_2_RX0_P	MGTFRXP0_227
678.3	115.9	Y4	FIREFLY_0_RX2_P	MGTFRXP2_229
679.4	116.1	AH4	FIREFLY_2_RX2_P	MGTFRXP2_227
679.5	116.2	AH3	FIREFLY_2_RX2_N	MGTFRXN2_227
688.1	117.6	AF8	FIREFLY_1_TX2_N	MGTFTXN2_228
688.2	117.6	AF9	FIREFLY_1_TX2_P	MGTFTXP2_228
695.0	118.8	AK8	FIREFLY_2_TX2_N	MGTFTXN2_227
695.2	118.8	AK9	FIREFLY_2_TX2_P	MGTFTXP2_227
703.9	120.3	AP3	FIREFLY_3_RX0_N	MGTFRXN0_226
704.1	120.4	AP4	FIREFLY_3_RX0_P	MGTFRXP0_226
706.0	120.7	AJ7	FIREFLY_2_TX3_P	MGTFTXP3_227
706.0	120.7	AJ6	FIREFLY_2_TX3_N	MGTFTXN3_227
709.4	121.3	AE6	FIREFLY_1_TX3_N	MGTFTXN3_228
709.6	121.3	AE7	FIREFLY_1_TX3_P	MGTFTXP3_228
709.8	121.3	AM3	FIREFLY_3_RX2_N	MGTFRXN2_226
710.0	121.4	AM4	FIREFLY_3_RX2_P	MGTFRXP2_226
715.8	122.4	AA7	FIREFLY_0_TX3_P	MGTFTXP3_229
716.2	122.4	AA6	FIREFLY_0_TX3_N	MGTFTXN3_229
718.6	122.8	AP8	FIREFLY_3_TX2_N	MGTFTXN2_226
718.6	122.8	AP9	FIREFLY_3_TX2_P	MGTFTXP2_226
724.7	123.9	AN6	FIREFLY_3_TX3_N	MGTFTXN3_226
724.9	123.9	AN7	FIREFLY_3_TX3_P	MGTFTXP3_226
725.7	124.1	AB8	FIREFLY_0_TX2_N	MGTFTXN2_229
725.8	124.1	AB9	FIREFLY_0_TX2_P	MGTFTXP2_229
763.6	130.5	AC7	FIREFLY_0_TX1_P	MGTFTXP1_229

Table 9 : Complete Pinout Table (continued on next page)

Trace Delay (ps)	Trace Length (mm)	Pin Number	Signal Name	Pin Name
763.8	130.6	AC6	FIREFLY_0_TX1_N	MGTFTXN1_229
765.1	130.8	AG7	FIREFLY_1_TX1_P	MGTFTXP1_228
765.3	130.8	AG6	FIREFLY_1_TX1_N	MGTFTXN1_228
768.6	131.4	AM9	FIREFLY_2_TX0_P	MGTFTXP0_227
768.8	131.4	AM8	FIREFLY_2_TX0_N	MGTFTXN0_227
770.0	131.6	AH9	FIREFLY_1_TX0_P	MGTFTXP0_228
770.0	131.6	AD9	FIREFLY_0_TX0_P	MGTFTXP0_229
770.2	131.7	AH8	FIREFLY_1_TX0_N	MGTFTXN0_228
770.3	131.7	AD8	FIREFLY_0_TX0_N	MGTFTXN0_229
771.2	131.8	AL7	FIREFLY_2_TX1_P	MGTFTXP1_227
771.4	131.9	AL6	FIREFLY_2_TX1_N	MGTFTXN1_227
784.4	134.1	AT9	FIREFLY_3_TX0_P	MGTFTXP0_226
784.5	134.1	AT8	FIREFLY_3_TX0_N	MGTFTXN0_226
792.2	135.4	AR6	FIREFLY_3_TX1_N	MGTFTXN1_226
792.2	135.4	AR7	FIREFLY_3_TX1_P	MGTFTXP1_226

Table 9 : Complete Pinout Table

Appendix B: Complete Pinout Table

Pin Number	Signal Name	Pin Name	Bank Voltage
BF23	AVR_B2U_1V8	IO_L2P_T0L_N2_66	1.8 (LVCMOS18)
BA24	AVR_MON_CLK_1V8	IO_L12P_T1U_N10_GC_66	1.8 (LVCMOS18)
BF22	AVR_U2B_1V8	IO_L2N_T0L_N3_66	1.8 (LVCMOS18)
BF12	CCLK	CCLK_0	1.8 (LVCMOS18)
BA12	DONE_1V8	DONE_0	1.8 (LVCMOS18)
AP20	EMCCLK_B	IO_L24P_T3U_N10_EMCCLK_65	1.8 (LVCMOS18)
BB34	FIREFLY_0_INT_1V8_L	IO_L14P_T2L_N2_GC_68	1.8 (LVCMOS18)
BE32	FIREFLY_0_MODPRS_L	IO_L3P_T0L_N4_AD15P_68	1.8 (LVCMOS18)
BB35	FIREFLY_0_RST_1V8_L	IO_L14N_T2L_N3_GC_68	1.8 (LVCMOS18)
AB3	FIREFLY_0_RX0_N	MGTFRXN0_229	MGT
AB4	FIREFLY_0_RX0_P	MGTFRXP0_229	MGT
AA1	FIREFLY_0_RX1_N	MGTFRXN1_229	MGT
AA2	FIREFLY_0_RX1_P	MGTFRXP1_229	MGT
Y3	FIREFLY_0_RX2_N	MGTFRXN2_229	MGT
Y4	FIREFLY_0_RX2_P	MGTFRXP2_229	MGT
W1	FIREFLY_0_RX3_N	MGTFRXN3_229	MGT
W2	FIREFLY_0_RX3_P	MGTFRXP3_229	MGT
BB32	FIREFLY_0_SCL_1V8	IO_L15N_T2L_N5_AD11N_68	1.8 (LVCMOS18)
BA32	FIREFLY_0_SDA_1V8	IO_L15P_T2L_N4_AD11P_68	1.8 (LVCMOS18)
AD8	FIREFLY_0_TX0_N	MGTFTXN0_229	MGT
AD9	FIREFLY_0_TX0_P	MGTFTXP0_229	MGT
AC6	FIREFLY_0_TX1_N	MGTFTXN1_229	MGT
AC7	FIREFLY_0_TX1_P	MGTFTXP1_229	MGT
AB8	FIREFLY_0_TX2_N	MGTFTXN2_229	MGT
AB9	FIREFLY_0_TX2_P	MGTFTXP2_229	MGT
AA6	FIREFLY_0_TX3_N	MGTFTXN3_229	MGT
AA7	FIREFLY_0_TX3_P	MGTFTXP3_229	MGT
AY32	FIREFLY_1_INT_1V8_L	IO_L16P_T2U_N6_QBC_AD3P_68	1.8 (LVCMOS18)
BF32	FIREFLY_1_MODPRS_L	IO_L3N_T0L_N5_AD15N_68	1.8 (LVCMOS18)
BA33	FIREFLY_1_RST_1V8_L	IO_L16N_T2U_N7_QBC_AD3N_68	1.8 (LVCMOS18)
AF3	FIREFLY_1_RX0_N	MGTFRXN0_228	MGT
AF4	FIREFLY_1_RX0_P	MGTFRXP0_228	MGT
AE1	FIREFLY_1_RX1_N	MGTFRXN1_228	MGT

Table 10 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
AE2	FIREFLY_1_RX1_P	MGTFRXP1_228	MGT
AD3	FIREFLY_1_RX2_N	MGTFRXN2_228	MGT
AD4	FIREFLY_1_RX2_P	MGTFRXP2_228	MGT
AC1	FIREFLY_1_RX3_N	MGTFRXN3_228	MGT
AC2	FIREFLY_1_RX3_P	MGTFRXP3_228	MGT
AY35	FIREFLY_1_SCL_1V8	IO_L17N_T2U_N9_AD10N_68	1.8 (LVCMOS18)
AW35	FIREFLY_1_SDA_1V8	IO_L17P_T2U_N8_AD10P_68	1.8 (LVCMOS18)
AH8	FIREFLY_1_TX0_N	MGTFTXN0_228	MGT
AH9	FIREFLY_1_TX0_P	MGTFTXP0_228	MGT
AG6	FIREFLY_1_TX1_N	MGTFTXN1_228	MGT
AG7	FIREFLY_1_TX1_P	MGTFTXP1_228	MGT
AF8	FIREFLY_1_TX2_N	MGTFTXN2_228	MGT
AF9	FIREFLY_1_TX2_P	MGTFTXP2_228	MGT
AE6	FIREFLY_1_TX3_N	MGTFTXN3_228	MGT
AE7	FIREFLY_1_TX3_P	MGTFTXP3_228	MGT
AW36	FIREFLY_2_INT_1V8_L	IO_L18P_T2U_N10_AD2P_68	1.8 (LVCMOS18)
BD31	FIREFLY_2_MODPRS_L	IO_L4P_T0U_N6_DBC_AD7P_68	1.8 (LVCMOS18)
AY36	FIREFLY_2_RST_1V8_L	IO_L18N_T2U_N11_AD2N_68	1.8 (LVCMOS18)
AK3	FIREFLY_2_RX0_N	MGTFRXN0_227	MGT
AK4	FIREFLY_2_RX0_P	MGTFRXP0_227	MGT
AJ1	FIREFLY_2_RX1_N	MGTFRXN1_227	MGT
AJ2	FIREFLY_2_RX1_P	MGTFRXP1_227	MGT
AH3	FIREFLY_2_RX2_N	MGTFRXN2_227	MGT
AH4	FIREFLY_2_RX2_P	MGTFRXP2_227	MGT
AG1	FIREFLY_2_RX3_N	MGTFRXN3_227	MGT
AG2	FIREFLY_2_RX3_P	MGTFRXP3_227	MGT
AW33	FIREFLY_2_SCL_1V8	IO_L19P_T3L_N0_DBC_AD9P_68	1.8 (LVCMOS18)
BA34	FIREFLY_2_SDA_1V8	IO_T2U_N12_68	1.8 (LVCMOS18)
AM8	FIREFLY_2_TX0_N	MGTFTXN0_227	MGT
AM9	FIREFLY_2_TX0_P	MGTFTXP0_227	MGT
AL6	FIREFLY_2_TX1_N	MGTFTXN1_227	MGT
AL7	FIREFLY_2_TX1_P	MGTFTXP1_227	MGT
AK8	FIREFLY_2_TX2_N	MGTFTXN2_227	MGT
AK9	FIREFLY_2_TX2_P	MGTFTXP2_227	MGT
AJ6	FIREFLY_2_TX3_N	MGTFTXN3_227	MGT
AJ7	FIREFLY_2_TX3_P	MGTFTXP3_227	MGT

Table 10 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
AY33	FIREFLY_3_INT_1V8_L	IO_L19N_T3L_N1_DBC_AD9N_68	1.8 (LVCMOS18)
BE31	FIREFLY_3_MODPRS_L	IO_L4N_T0U_N7_DBC_AD7N_68	1.8 (LVCMOS18)
AV33	FIREFLY_3_RST_1V8_L	IO_L20P_T3L_N2_AD1P_68	1.8 (LVCMOS18)
AP3	FIREFLY_3_RX0_N	MGTFRXN0_226	MGT
AP4	FIREFLY_3_RX0_P	MGTFRXP0_226	MGT
AN1	FIREFLY_3_RX1_N	MGTFRXN1_226	MGT
AN2	FIREFLY_3_RX1_P	MGTFRXP1_226	MGT
AM3	FIREFLY_3_RX2_N	MGTFRXN2_226	MGT
AM4	FIREFLY_3_RX2_P	MGTFRXP2_226	MGT
AL1	FIREFLY_3_RX3_N	MGTFRXN3_226	MGT
AL2	FIREFLY_3_RX3_P	MGTFRXP3_226	MGT
AU32	FIREFLY_3_SCL_1V8	IO_L21P_T3L_N4_AD8P_68	1.8 (LVCMOS18)
AW34	FIREFLY_3_SDA_1V8	IO_L20N_T3L_N3_AD1N_68	1.8 (LVCMOS18)
AT8	FIREFLY_3_TX0_N	MGTFTXN0_226	MGT
AT9	FIREFLY_3_TX0_P	MGTFTXP0_226	MGT
AR6	FIREFLY_3_TX1_N	MGTFTXN1_226	MGT
AR7	FIREFLY_3_TX1_P	MGTFTXP1_226	MGT
AP8	FIREFLY_3_TX2_N	MGTFTXN2_226	MGT
AP9	FIREFLY_3_TX2_P	MGTFTXP2_226	MGT
AN6	FIREFLY_3_TX3_N	MGTFTXN3_226	MGT
AN7	FIREFLY_3_TX3_P	MGTFTXP3_226	MGT
AE10	FIREFLY_CLK_0_PIN_N	MGTREFCLK0N_228	MGT REFCLK
AE11	FIREFLY_CLK_0_PIN_P	MGTREFCLK0P_228	MGT REFCLK
AN10	FIREFLY_CLK_1_PIN_N	MGTREFCLK0N_226	MGT REFCLK
AN11	FIREFLY_CLK_1_PIN_P	MGTREFCLK0P_226	MGT REFCLK
BC11	FPGA_FLASH_CE0_L	RDWR_FCS_B_0	1.8 (LVCMOS18)
BF17	FPGA_FLASH_CE1_L	IO_L2N_T0L_N3_FWE_FCS2_B_65	1.8 (LVCMOS18)
BD13	FPGA_FLASH_DQ0	D00_MOSI_0	1.8 (LVCMOS18)
BE12	FPGA_FLASH_DQ1	D01_DIN_0	1.8 (LVCMOS18)
BD11	FPGA_FLASH_DQ2	D02_0	1.8 (LVCMOS18)
BE11	FPGA_FLASH_DQ3	D03_0	1.8 (LVCMOS18)
AU20	FPGA_FLASH_DQ4	IO_L22P_T3U_N6_DBC_AD0P-_D04_65	1.8 (LVCMOS18)
AU19	FPGA_FLASH_DQ5	IO_L22N_T3U_N7_DBC_AD0N-_D05_65	1.8 (LVCMOS18)
AR18	FPGA_FLASH_DQ6	IO_L21P_T3L_N4_AD8P_D06_65	1.8 (LVCMOS18)

Table 10 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
AT18	FPGA_FLASH_DQ7	IO_L21N_T3L_N5_AD8N_D07_65	1.8 (LVCMOS18)
AY31	GPIO_0_1V8_N	IO_L14N_T2L_N3_GC_67	1.8 (LVCMOS18)
AW30	GPIO_0_1V8_P	IO_L14P_T2L_N2_GC_67	1.8 (LVCMOS18)
AW31	GPIO_1_1V8_N	IO_L15N_T2L_N5_AD11N_67	1.8 (LVCMOS18)
AV31	GPIO_1_1V8_P	IO_L15P_T2L_N4_AD11P_67	1.8 (LVCMOS18)
AW29	GPIO_2_1V8_N	IO_L16N_T2U_N7_QBC_AD3N_67	1.8 (LVCMOS18)
AV29	GPIO_2_1V8_P	IO_L16P_T2U_N6_QBC_AD3P_67	1.8 (LVCMOS18)
AW28	GPIO_3_1V8_N	IO_L17N_T2U_N9_AD10N_67	1.8 (LVCMOS18)
AV28	GPIO_3_1V8_P	IO_L17P_T2U_N8_AD10P_67	1.8 (LVCMOS18)
AY13	INIT_B_1V8	INIT_B_0	1.8 (LVCMOS18)
AY28	ISO_CLK_1V8	IO_L13P_T2L_N0_GC_QBC_67	1.8 (LVCMOS18)
AV8	PCIE_LCL_REFCLK_PIN_N	MGTREFCLK0N_225	MGT REFCLK
AV9	PCIE_LCL_REFCLK_PIN_P	MGTREFCLK0P_225	MGT REFCLK
BB8	PCIE_REFCLK_PIN_N	MGTREFCLK0N_224	MGT REFCLK
BB9	PCIE_REFCLK_PIN_P	MGTREFCLK0P_224	MGT REFCLK
BC1	PCIE_RX0_N	MGTYRXN0_224	MGT
BC2	PCIE_RX0_P	MGTYRXP0_224	MGT
BB3	PCIE_RX1_N	MGTYRXN1_224	MGT
BB4	PCIE_RX1_P	MGTYRXP1_224	MGT
BA1	PCIE_RX2_N	MGTYRXN2_224	MGT
BA2	PCIE_RX2_P	MGTYRXP2_224	MGT
AY3	PCIE_RX3_N	MGTYRXN3_224	MGT
AY4	PCIE_RX3_P	MGTYRXP3_224	MGT
AW1	PCIE_RX4_N	MGTYRXN0_225	MGT
AW2	PCIE_RX4_P	MGTYRXP0_225	MGT
AV3	PCIE_RX5_N	MGTYRXN1_225	MGT
AV4	PCIE_RX5_P	MGTYRXP1_225	MGT
AU1	PCIE_RX6_N	MGTYRXN2_225	MGT
AU2	PCIE_RX6_P	MGTYRXP2_225	MGT
AT3	PCIE_RX7_N	MGTYRXN3_225	MGT
AT4	PCIE_RX7_P	MGTYRXP3_225	MGT
BF4	PCIE_TX0_PIN_N	MGTYTXN0_224	MGT
BF5	PCIE_TX0_PIN_P	MGTYTXP0_224	MGT
BF8	PCIE_TX1_PIN_N	MGTYTXN1_224	MGT
BF9	PCIE_TX1_PIN_P	MGTYTXP1_224	MGT
BE6	PCIE_TX2_PIN_N	MGTYTXN2_224	MGT

Table 10 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
BE7	PCIE_TX2_PIN_P	MGTYTXP2_224	MGT
BD4	PCIE_TX3_PIN_N	MGTYTXN3_224	MGT
BD5	PCIE_TX3_PIN_P	MGTYTXP3_224	MGT
BD8	PCIE_TX4_PIN_N	MGTYTXN0_225	MGT
BD9	PCIE_TX4_PIN_P	MGTYTXP0_225	MGT
BC6	PCIE_TX5_PIN_N	MGTYTXN1_225	MGT
BC7	PCIE_TX5_PIN_P	MGTYTXP1_225	MGT
BA6	PCIE_TX6_PIN_N	MGTYTXN2_225	MGT
BA7	PCIE_TX6_PIN_P	MGTYTXP2_225	MGT
AW6	PCIE_TX7_PIN_N	MGTYTXN3_225	MGT
AW7	PCIE_TX7_PIN_P	MGTYTXP3_225	MGT
AT19	PERST0_1V8_L	IO_T3U_N12_PERSTN0_65	1.8 (LVCMOS18)
BB11	PROGRAM_B_1V8	PROGRAM_B_0	1.8 (LVCMOS18)
BE33	QSFP_0_INT_1V8_L	IO_T0U_N12_VRP_68	1.8 (LVCMOS18)
BD34	QSFP_0_LPMODE_1V8	IO_L6N_T0U_N11_AD6N_68	1.8 (LVCMOS18)
BE35	QSFP_0_MODPRS_L	IO_L1P_T0L_N0_DBC_68	1.8 (LVCMOS18)
BC33	QSFP_0_RST_1V8_L	IO_L6P_T0U_N10_AD6P_68	1.8 (LVCMOS18)
K44	QSFP_0_RX0_N	MGTFRXN0_132	MGT
K43	QSFP_0_RX0_P	MGTFRXP0_132	MGT
J46	QSFP_0_RX1_N	MGTFRXN1_132	MGT
J45	QSFP_0_RX1_P	MGTFRXP1_132	MGT
H44	QSFP_0_RX2_N	MGTFRXN2_132	MGT
H43	QSFP_0_RX2_P	MGTFRXP2_132	MGT
G46	QSFP_0_RX3_N	MGTFRXN3_132	MGT
G45	QSFP_0_RX3_P	MGTFRXP3_132	MGT
F44	QSFP_0_RX4_N	MGTFRXN0_133	MGT
F43	QSFP_0_RX4_P	MGTFRXP0_133	MGT
E46	QSFP_0_RX5_N	MGTFRXN1_133	MGT
E45	QSFP_0_RX5_P	MGTFRXP1_133	MGT
D44	QSFP_0_RX6_N	MGTFRXN2_133	MGT
D43	QSFP_0_RX6_P	MGTFRXP2_133	MGT
B44	QSFP_0_RX7_N	MGTFRXN3_133	MGT
B43	QSFP_0_RX7_P	MGTFRXP3_133	MGT
BC32	QSFP_0_SCL_1V8	IO_L5P_T0U_N8_AD14P_68	1.8 (LVCMOS18)
BD33	QSFP_0_SDA_1V8	IO_L5N_T0U_N9_AD14N_68	1.8 (LVCMOS18)
M39	QSFP_0_TX0_N	MGTFTXN0_132	MGT

Table 10 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
M38	QSFP_0_TX0_P	MGTFTXP0_132	MGT
L41	QSFP_0_TX1_N	MGTFTXN1_132	MGT
L40	QSFP_0_TX1_P	MGTFTXP1_132	MGT
K39	QSFP_0_TX2_N	MGTFTXN2_132	MGT
K38	QSFP_0_TX2_P	MGTFTXP2_132	MGT
J41	QSFP_0_TX3_N	MGTFTXN3_132	MGT
J40	QSFP_0_TX3_P	MGTFTXP3_132	MGT
G41	QSFP_0_TX4_N	MGTFTXN0_133	MGT
G40	QSFP_0_TX4_P	MGTFTXP0_133	MGT
E41	QSFP_0_TX5_N	MGTFTXN1_133	MGT
E40	QSFP_0_TX5_P	MGTFTXP1_133	MGT
C41	QSFP_0_TX6_N	MGTFTXN2_133	MGT
C40	QSFP_0_TX6_P	MGTFTXP2_133	MGT
A41	QSFP_0_TX7_N	MGTFTXN3_133	MGT
A40	QSFP_0_TX7_P	MGTFTXP3_133	MGT
BC38	QSFP_1_INT_1V8_L	IO_L9P_T1L_N4_AD12P_68	1.8 (LVCMOS18)
BF38	QSFP_1_LPMODE_1V8	IO_L8N_T1L_N3_AD5N_68	1.8 (LVCMOS18)
BF35	QSFP_1_MODPRS_L	IO_L1N_T0L_N1_DBC_68	1.8 (LVCMOS18)
BE38	QSFP_1_RST_1V8_L	IO_L8P_T1L_N2_AD5P_68	1.8 (LVCMOS18)
P44	QSFP_1_RX0_N	MGTFRXN0_131	MGT
P43	QSFP_1_RX0_P	MGTFRXP0_131	MGT
N46	QSFP_1_RX1_N	MGTFRXN1_131	MGT
N45	QSFP_1_RX1_P	MGTFRXP1_131	MGT
M44	QSFP_1_RX2_N	MGTFRXN2_131	MGT
M43	QSFP_1_RX2_P	MGTFRXP2_131	MGT
L46	QSFP_1_RX3_N	MGTFRXN3_131	MGT
L45	QSFP_1_RX3_P	MGTFRXP3_131	MGT
V44	QSFP_1_RX4_N	MGTFRXN0_130	MGT
V43	QSFP_1_RX4_P	MGTFRXP0_130	MGT
U46	QSFP_1_RX5_N	MGTFRXN1_130	MGT
U45	QSFP_1_RX5_P	MGTFRXP1_130	MGT
T44	QSFP_1_RX6_N	MGTFRXN2_130	MGT
T43	QSFP_1_RX6_P	MGTFRXP2_130	MGT
R46	QSFP_1_RX7_N	MGTFRXN3_130	MGT
R45	QSFP_1_RX7_P	MGTFRXP3_130	MGT
BE37	QSFP_1_SCL_1V8	IO_L7P_T1L_N0_QBC_AD13P_68	1.8 (LVCMOS18)

Table 10 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
BF37	QSFP_1_SDA_1V8	IO_L7N_T1L_N1_QBC_AD13N_68	1.8 (LVCMOS18)
T39	QSFP_1_TX0_N	MGTFTXN0_131	MGT
T38	QSFP_1_TX0_P	MGTFTXP0_131	MGT
R41	QSFP_1_TX1_N	MGTFTXN1_131	MGT
R40	QSFP_1_TX1_P	MGTFTXP1_131	MGT
P39	QSFP_1_TX2_N	MGTFTXN2_131	MGT
P38	QSFP_1_TX2_P	MGTFTXP2_131	MGT
N41	QSFP_1_TX3_N	MGTFTXN3_131	MGT
N40	QSFP_1_TX3_P	MGTFTXP3_131	MGT
Y39	QSFP_1_TX4_N	MGTFTXN0_130	MGT
Y38	QSFP_1_TX4_P	MGTFTXP0_130	MGT
W41	QSFP_1_TX5_N	MGTFTXN1_130	MGT
W40	QSFP_1_TX5_P	MGTFTXP1_130	MGT
V39	QSFP_1_TX6_N	MGTFTXN2_130	MGT
V38	QSFP_1_TX6_P	MGTFTXP2_130	MGT
U41	QSFP_1_TX7_N	MGTFTXN3_130	MGT
U40	QSFP_1_TX7_P	MGTFTXP3_130	MGT
BB36	QSFP_2_INT_1V8_L	IO_L13N_T2L_N1_GC_QBC_68	1.8 (LVCMOS18)
BA35	QSFP_2_LPMODE_1V8	IO_L13P_T2L_N0_GC_QBC_68	1.8 (LVCMOS18)
BF34	QSFP_2_MODPRS_L	IO_L2N_T0L_N3_68	1.8 (LVCMOS18)
BE36	QSFP_2_RST_1V8_L	IO_T1U_N12_68	1.8 (LVCMOS18)
AP44	QSFP_2_RX0_N	MGTFRXN0_126	MGT
AP43	QSFP_2_RX0_P	MGTFRXP0_126	MGT
AN46	QSFP_2_RX1_N	MGTFRXN1_126	MGT
AN45	QSFP_2_RX1_P	MGTFRXP1_126	MGT
AM44	QSFP_2_RX2_N	MGTFRXN2_126	MGT
AM43	QSFP_2_RX2_P	MGTFRXP2_126	MGT
AL46	QSFP_2_RX3_N	MGTFRXN3_126	MGT
AL45	QSFP_2_RX3_P	MGTFRXP3_126	MGT
AK44	QSFP_2_RX4_N	MGTFRXN0_127	MGT
AK43	QSFP_2_RX4_P	MGTFRXP0_127	MGT
AJ46	QSFP_2_RX5_N	MGTFRXN1_127	MGT
AJ45	QSFP_2_RX5_P	MGTFRXP1_127	MGT
AH44	QSFP_2_RX6_N	MGTFRXN2_127	MGT
AH43	QSFP_2_RX6_P	MGTFRXP2_127	MGT
AG46	QSFP_2_RX7_N	MGTFRXN3_127	MGT

Table 10 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
AG45	QSFP_2_RX7_P	MGTFRXP3_127	MGT
BC36	QSFP_2_SCL_1V8	IO_L12P_T1U_N10_GC_68	1.8 (LVCMOS18)
BD36	QSFP_2_SDA_1V8	IO_L12N_T1U_N11_GC_68	1.8 (LVCMOS18)
AT39	QSFP_2_TX0_N	MGTFTXN0_126	MGT
AT38	QSFP_2_TX0_P	MGTFTXP0_126	MGT
AR41	QSFP_2_TX1_N	MGTFTXN1_126	MGT
AR40	QSFP_2_TX1_P	MGTFTXP1_126	MGT
AP39	QSFP_2_TX2_N	MGTFTXN2_126	MGT
AP38	QSFP_2_TX2_P	MGTFTXP2_126	MGT
AN41	QSFP_2_TX3_N	MGTFTXN3_126	MGT
AN40	QSFP_2_TX3_P	MGTFTXP3_126	MGT
AM39	QSFP_2_TX4_N	MGTFTXN0_127	MGT
AM38	QSFP_2_TX4_P	MGTFTXP0_127	MGT
AL41	QSFP_2_TX5_N	MGTFTXN1_127	MGT
AL40	QSFP_2_TX5_P	MGTFTXP1_127	MGT
AK39	QSFP_2_TX6_N	MGTFTXN2_127	MGT
AK38	QSFP_2_TX6_P	MGTFTXP2_127	MGT
AJ41	QSFP_2_TX7_N	MGTFTXN3_127	MGT
AJ40	QSFP_2_TX7_P	MGTFTXP3_127	MGT
BD35	QSFP_3_INT_1V8_L	IO_L11N_T1U_N9_GC_68	1.8 (LVCMOS18)
BC34	QSFP_3_LPMODE_1V8	IO_L11P_T1U_N8_GC_68	1.8 (LVCMOS18)
BF33	QSFP_3_MODPRS_L	IO_L2P_T0L_N2_68	1.8 (LVCMOS18)
BC37	QSFP_3_RST_1V8_L	IO_L10N_T1U_N7_QBC_AD4N_68	1.8 (LVCMOS18)
BC46	QSFP_3_RX0_N	MGTFRXN0_124	MGT
BC45	QSFP_3_RX0_P	MGTFRXP0_124	MGT
BA46	QSFP_3_RX1_N	MGTFRXN1_124	MGT
BA45	QSFP_3_RX1_P	MGTFRXP1_124	MGT
AY44	QSFP_3_RX2_N	MGTFRXN2_124	MGT
AY43	QSFP_3_RX2_P	MGTFRXP2_124	MGT
AW46	QSFP_3_RX3_N	MGTFRXN3_124	MGT
AW45	QSFP_3_RX3_P	MGTFRXP3_124	MGT
AV44	QSFP_3_RX4_N	MGTFRXN0_125	MGT
AV43	QSFP_3_RX4_P	MGTFRXP0_125	MGT
AU46	QSFP_3_RX5_N	MGTFRXN1_125	MGT
AU45	QSFP_3_RX5_P	MGTFRXP1_125	MGT
AT44	QSFP_3_RX6_N	MGTFRXN2_125	MGT

Table 10 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
AT43	QSFP_3_RX6_P	MGTFRXP2_125	MGT
AR46	QSFP_3_RX7_N	MGTFRXN3_125	MGT
AR45	QSFP_3_RX7_P	MGTFRXP3_125	MGT
BD38	QSFP_3_SCL_1V8	IO_L9N_T1L_N5_AD12N_68	1.8 (LVCMOS18)
BB37	QSFP_3_SDA_1V8	IO_L10P_T1U_N6_QBC_AD4P_68	1.8 (LVCMOS18)
BF43	QSFP_3_TX0_N	MGTFTXN0_124	MGT
BF42	QSFP_3_TX0_P	MGTFTXP0_124	MGT
BE41	QSFP_3_TX1_N	MGTFTXN1_124	MGT
BE40	QSFP_3_TX1_P	MGTFTXP1_124	MGT
BD43	QSFP_3_TX2_N	MGTFTXN2_124	MGT
BD42	QSFP_3_TX2_P	MGTFTXP2_124	MGT
BC41	QSFP_3_TX3_N	MGTFTXN3_124	MGT
BC40	QSFP_3_TX3_P	MGTFTXP3_124	MGT
BB43	QSFP_3_TX4_N	MGTFTXN0_125	MGT
BB42	QSFP_3_TX4_P	MGTFTXP0_125	MGT
BA41	QSFP_3_TX5_N	MGTFTXN1_125	MGT
BA40	QSFP_3_TX5_P	MGTFTXP1_125	MGT
AW41	QSFP_3_TX6_N	MGTFTXN2_125	MGT
AW40	QSFP_3_TX6_P	MGTFTXP2_125	MGT
AU41	QSFP_3_TX7_N	MGTFTXN3_125	MGT
AU40	QSFP_3_TX7_P	MGTFTXP3_125	MGT
H39	QSFP_CLK_0_PIN_N	MGTREFCLK0N_132	MGT REFCLK
H38	QSFP_CLK_0_PIN_P	MGTREFCLK0P_132	MGT REFCLK
R37	QSFP_CLK_1_PIN_N	MGTREFCLK0N_130	MGT REFCLK
R36	QSFP_CLK_1_PIN_P	MGTREFCLK0P_130	MGT REFCLK
AG37	QSFP_CLK_2_PIN_N	MGTREFCLK0N_127	MGT REFCLK
AG36	QSFP_CLK_2_PIN_P	MGTREFCLK0P_127	MGT REFCLK
AU37	QSFP_CLK_3_PIN_N	MGTREFCLK0N_125	MGT REFCLK
AU36	QSFP_CLK_3_PIN_P	MGTREFCLK0P_125	MGT REFCLK
AY22	REFCLK200_PIN_N	IO_L13N_T2L_N1_GC_QBC_66	1.8 (LVDS)
AW23	REFCLK200_PIN_P	IO_L13P_T2L_N0_GC_QBC_66	1.8 (LVDS)
AU26	SI5328_0_1V8_INT_C1B	IO_L19P_T3L_N0_DBC_AD9P_67	1.8 (LVCMOS18)
AV26	SI5328_0_1V8_LOL	IO_L19N_T3L_N1_DBC_AD9N_67	1.8 (LVCMOS18)
BC27	SI5328_0_CLKIN1_N	IO_L11N_T1U_N9_GC_67	1.8 (LVCMOS18)
BB27	SI5328_0_CLKIN1_P	IO_L11P_T1U_N8_GC_67	1.8 (LVCMOS18)
J37	SI5328_0_CLKIN2_N	MGTREFCLK1N_131	MGT REFCLK

Table 10 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
J36	SI5328_0_CLKIN2_P	MGTREFCLK1P_131	MGT REFCLK
D39	SI5328_0_CLKOUT1_PIN_N	MGTREFCLK0N_133	MGT REFCLK
D38	SI5328_0_CLKOUT1_PIN_P	MGTREFCLK0P_133	MGT REFCLK
L37	SI5328_0_CLKOUT2_PIN_N	MGTREFCLK0N_131	MGT REFCLK
L36	SI5328_0_CLKOUT2_PIN_P	MGTREFCLK0P_131	MGT REFCLK
AR27	SI5328_0_RST_1V8_L	IO_L24P_T3U_N10_67	1.8 (LVCMOS18)
AU27	SI5328_1_1V8_INT_C1B	IO_L20P_T3L_N2_AD1P_67	1.8 (LVCMOS18)
AV27	SI5328_1_1V8_LOL	IO_L20N_T3L_N3_AD1N_67	1.8 (LVCMOS18)
BA28	SI5328_1_CLKIN1_N	IO_L12N_T1U_N11_GC_67	1.8 (LVDS)
BA27	SI5328_1_CLKIN1_P	IO_L12P_T1U_N10_GC_67	1.8 (LVDS)
AJ37	SI5328_1_CLKIN2_N	MGTREFCLK1N_126	MGT REFCLK
AJ36	SI5328_1_CLKIN2_P	MGTREFCLK1P_126	MGT REFCLK
AL37	SI5328_1_CLKOUT1_PIN_N	MGTREFCLK0N_126	MGT REFCLK
AL36	SI5328_1_CLKOUT1_PIN_P	MGTREFCLK0P_126	MGT REFCLK
AY39	SI5328_1_CLKOUT2_PIN_N	MGTREFCLK0N_124	MGT REFCLK
AY38	SI5328_1_CLKOUT2_PIN_P	MGTREFCLK0P_124	MGT REFCLK
AT27	SI5328_1_RST_1V8_L	IO_L24N_T3U_N11_67	1.8 (LVCMOS18)
AT28	SI5328_1V8_SCL	IO_L23N_T3U_N9_67	1.8 (LVCMOS18)
AR28	SI5328_1V8_SDA	IO_L23P_T3U_N8_67	1.8 (LVCMOS18)
AT30	SI5328_2_1V8_INT_C1B	IO_L21P_T3L_N4_AD8P_67	1.8 (LVCMOS18)
AU31	SI5328_2_1V8_LOL	IO_L21N_T3L_N5_AD8N_67	1.8 (LVCMOS18)
BB30	SI5328_2_CLKIN1_N	IO_L10N_T1U_N7_QBC_AD4N_67	1.8 (LVDS)
BB29	SI5328_2_CLKIN1_P	IO_L10P_T1U_N6_QBC_AD4P_67	1.8 (LVDS)
W10	SI5328_2_CLKIN2_N	MGTREFCLK1N_229	MGT REFCLK
W11	SI5328_2_CLKIN2_P	MGTREFCLK1P_229	MGT REFCLK
AA10	SI5328_2_CLKOUT1_PIN_N	MGTREFCLK0N_229	MGT REFCLK
AA11	SI5328_2_CLKOUT1_PIN_P	MGTREFCLK0P_229	MGT REFCLK
AJ10	SI5328_2_CLKOUT2_PIN_N	MGTREFCLK0N_227	MGT REFCLK
AJ11	SI5328_2_CLKOUT2_PIN_P	MGTREFCLK0P_227	MGT REFCLK
BE25	SPARE_SCL	IO_L5N_T0U_N9_AD14N_66	1.8 (LVCMOS18)
BC23	SPARE_SDA	IO_L6P_T0U_N10_AD6P_66	1.8 (LVCMOS18)
BD23	SPARE_WP	IO_L6N_T0U_N11_AD6N_66	1.8 (LVCMOS18)
BD21	SRVC_MD_L_1V8	IO_L3P_T0L_N4_AD15P_66	1.8 (LVCMOS18)
BF13	TCK	TCK_0	1.8 (LVCMOS18)
BC13	TDI	TDI_0	1.8 (LVCMOS18)
BB12	TDO	TDO_0	1.8 (LVCMOS18)

Table 10 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	Bank Voltage
BE13	TMS	TMS_0	1.8 (LVCMOS18)
AU25	USER_LED_G0_1V8	IO_L16P_T2U_N6_QBC_AD3P_66	1.8 (LVCMOS18)
AU24	USER_LED_G1_1V8	IO_L16N_T2U_N7_QBC_AD3N_66	1.8 (LVCMOS18)
AV23	USER_LED_G2_1V8	IO_L17P_T2U_N8_AD10P_66	1.8 (LVCMOS18)
AV22	USER_LED_G3_1V8	IO_L17N_T2U_N9_AD10N_66	1.8 (LVCMOS18)
AU21	USER_LED_G4_1V8	IO_L18P_T2U_N10_AD2P_66	1.8 (LVCMOS18)
AV21	USER_LED_G5_1V8	IO_L18N_T2U_N11_AD2N_66	1.8 (LVCMOS18)
AP24	USR_SW_0	IO_L22N_T3U_N7_DBC_AD0N_66	1.8 (LVCMOS18)
AP23	USR_SW_1	IO_L23P_T3U_N8_66	1.8 (LVCMOS18)

Table 10 : Complete Pinout Table

Revision History

Date	Revision	Changed By	Nature of Change
12-Oct-2023	1.0	K. Roth	Initial Release

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